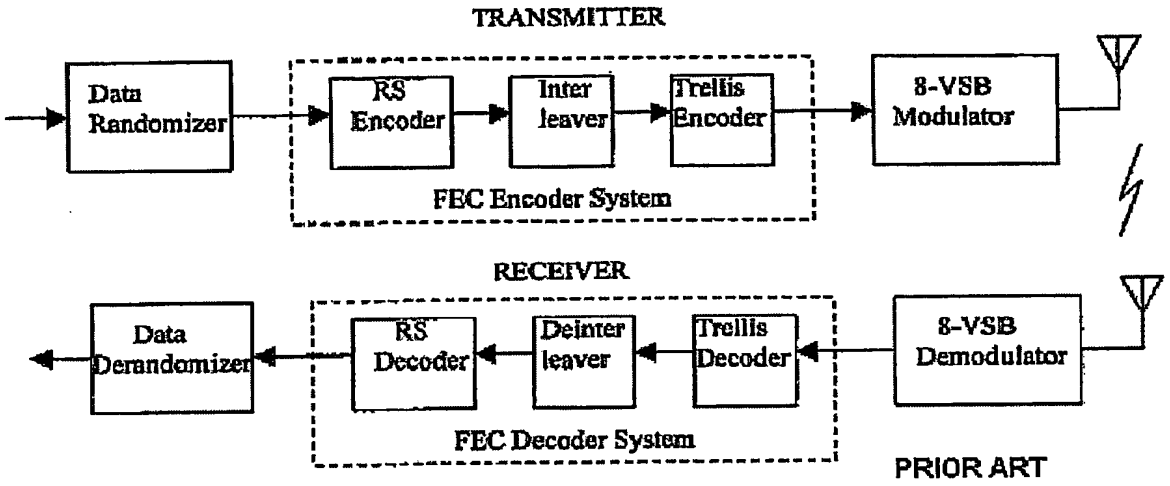

TRANSMITTER
Data Randomizer
RS Encoder
Inter leaver
Trellis Encoder
FEC Encoder System
8-VSB Modulator
RECEIVER
Data Derandomizer
RS Decoder
Deinter leaver
Trellis Decoder
FEC Decoder System
8-VSB Demodulator
PRIOR ART

Fig. 1 -

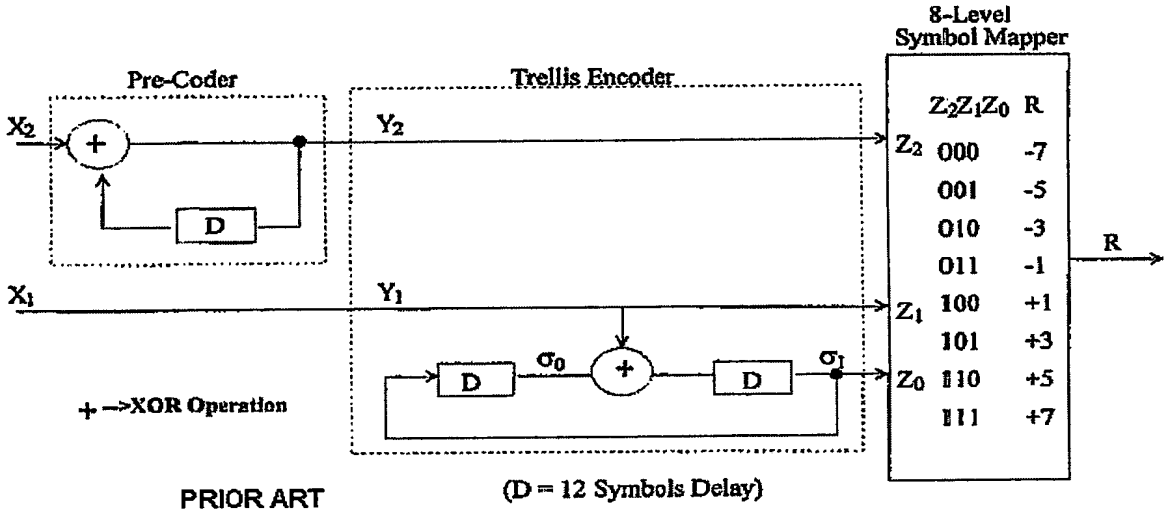

8-Level Symbol Mapper
Pre-Coder
Trellis Encoder
X2
Y2
D
X1
Y1
D
σ0
D
σ1
+ —>XOR Operation
Z2Z1Z0 R
Z2 000 -7
001 -5
010 -3
011 -1
Z1 100 +1
101 +3
Z0 110 +5
111 +7
R
PRIOR ART
(D = 12 Symbols Delay)

Fig. 2

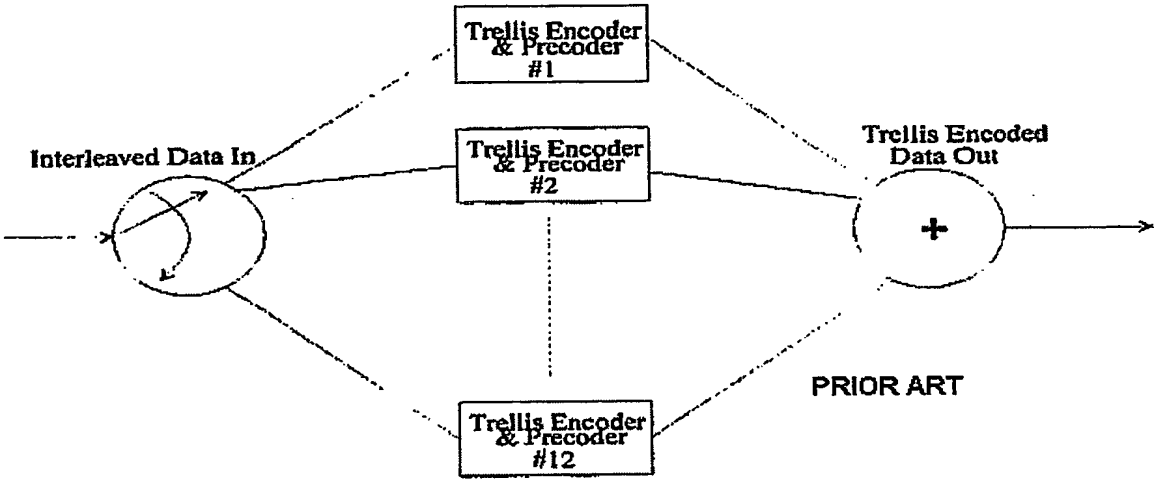

Trellis Encoder & Precoder #1
Interleaved Data In
Trellis Encoder & Precoder #2
Trellis Encoded Data Out
+
Trellis Encoder & Precoder #12
PRIOR ART

Fig. 3

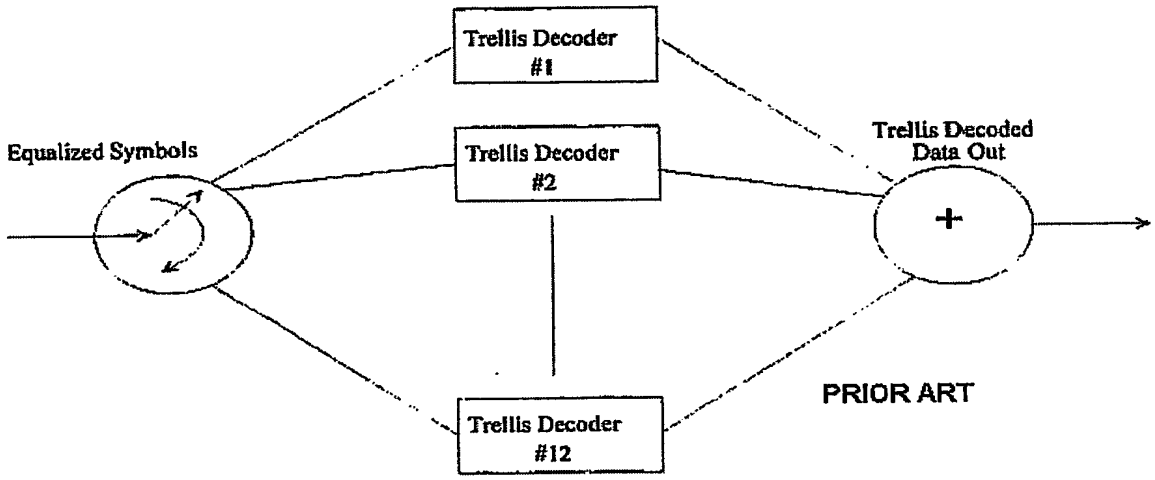

Trellis Decoder #1
Equalized Symbols
Trellis Decoder #2
Trellis Decoded Data Out
+
Trellis Decoder #12
PRIOR ART

Fig. 4

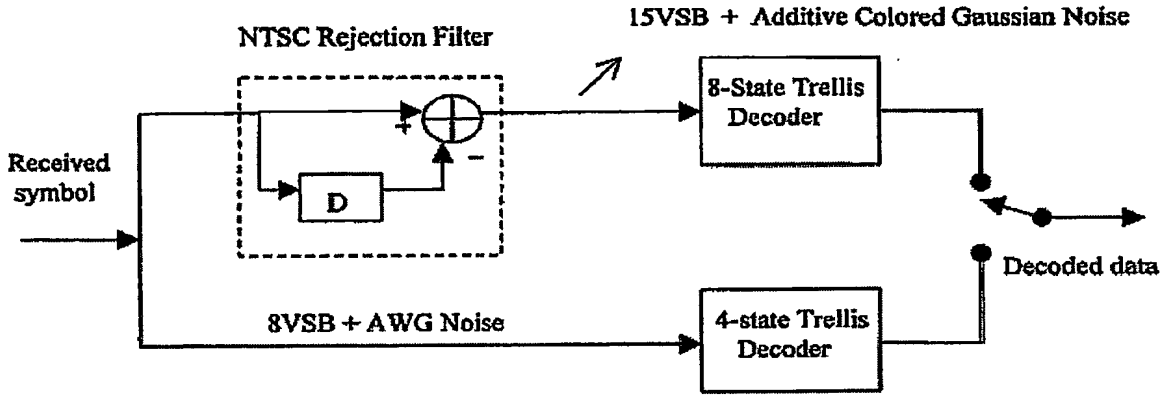

NTSC Rejection Filter
15VSB + Additive Colored Gaussian Noise
Received symbol
D
+
-
8-State Trellis Decoder
Decoded data
8VSB + AWG Noise
4-state Trellis Decoder
D = 1 symbol delay for each of the 12 decoders
PRIOR ART

Fig. 5

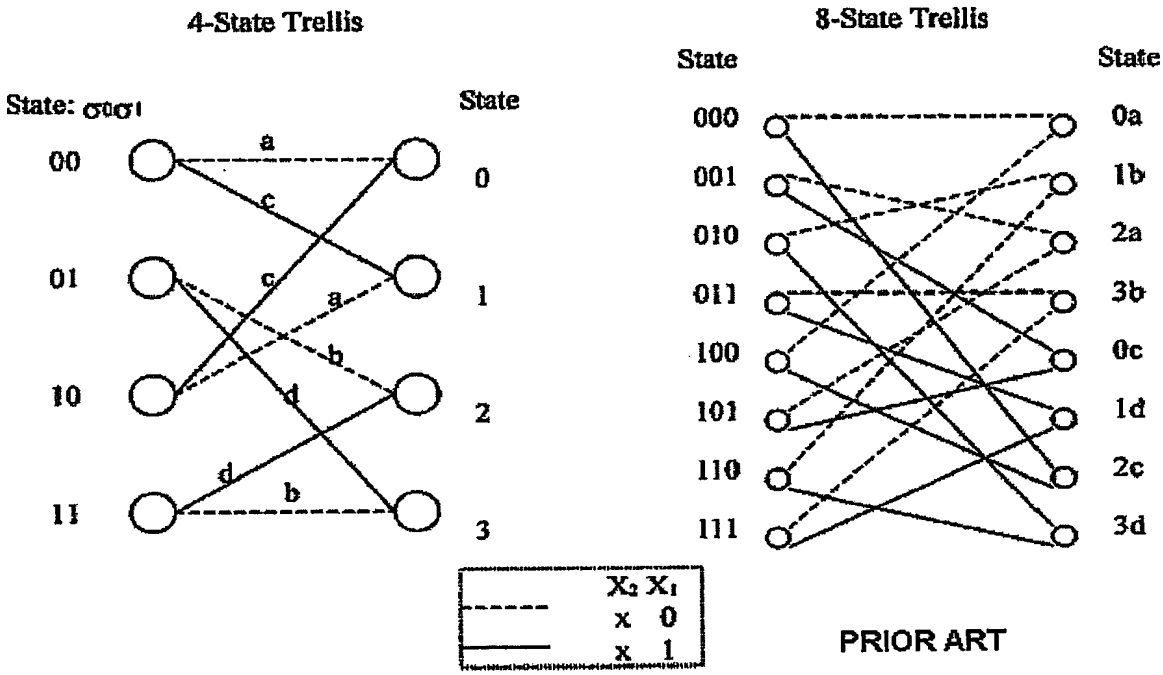
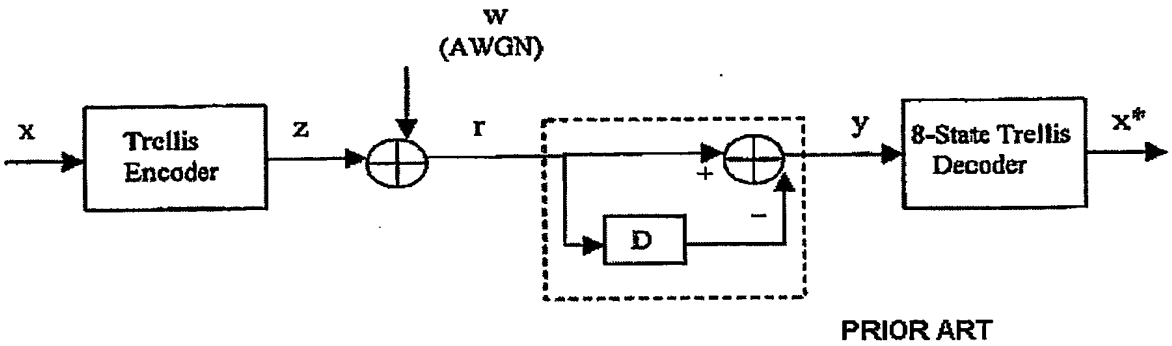

4-State Trellis
State: σ0σ1
State
00
01
10
11
0
1
2
3
a
b
c
d
8-State Trellis
State
State
000
001
010
011
100
101
110
111
0a
1b
2a
3b
0c
1d
2c
3d
X2 X1
x 0
x 1
PRIOR ART

Fig. 6



D = 1 symbol delay for each of the 12 decoders

Fig. 7

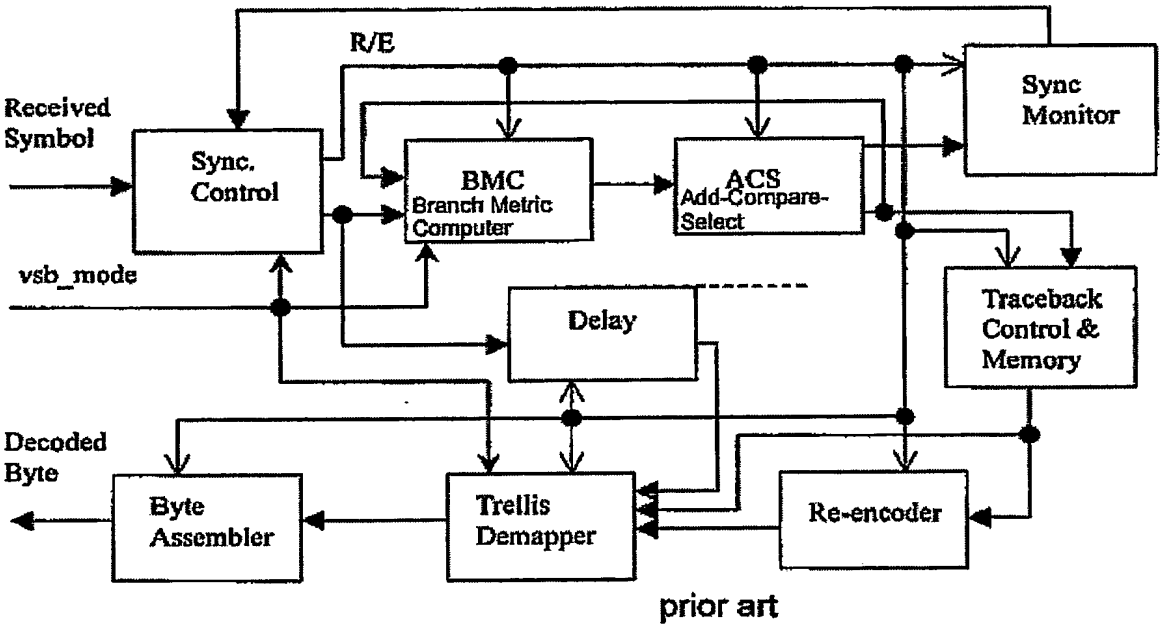


Fig. 8

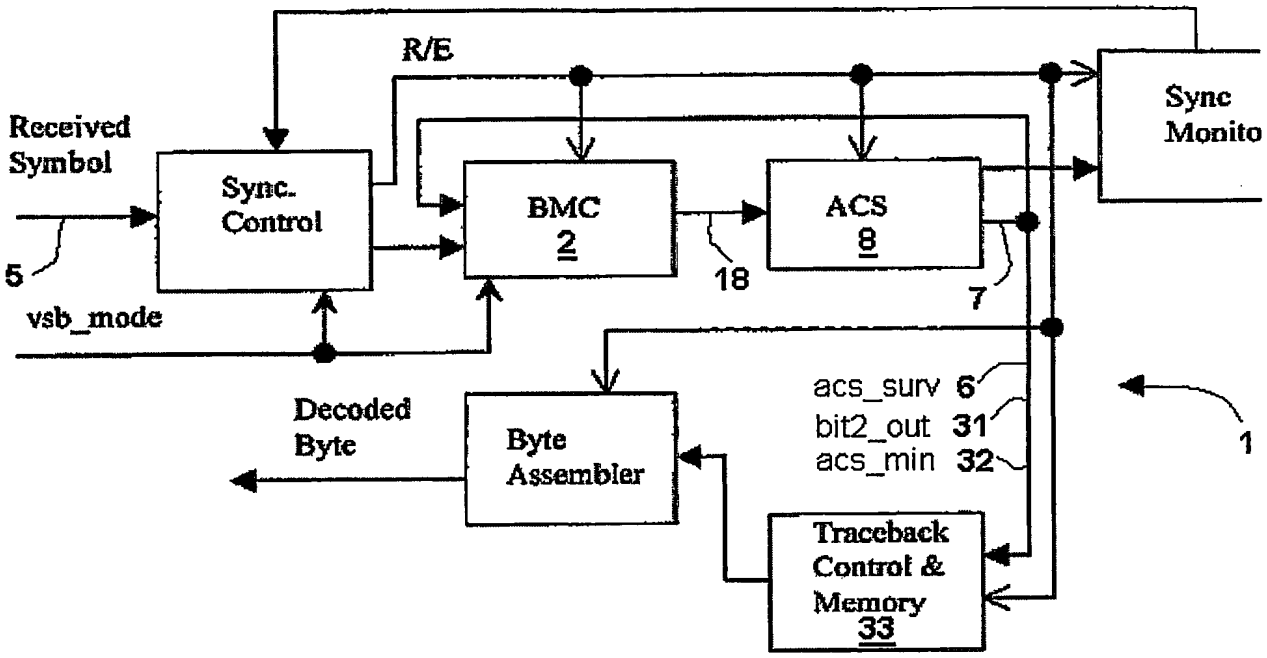

R/E
Received Symbol
Sync. Control
BMC 2
ACS 8
Sync Monito
5
18
7
vsb_mode
acs_surv 6
bit2_out 31
acs_min 32
1
Decoded Byte
Byte Assembler
Traceback Control & Memory 33

Fig. 9

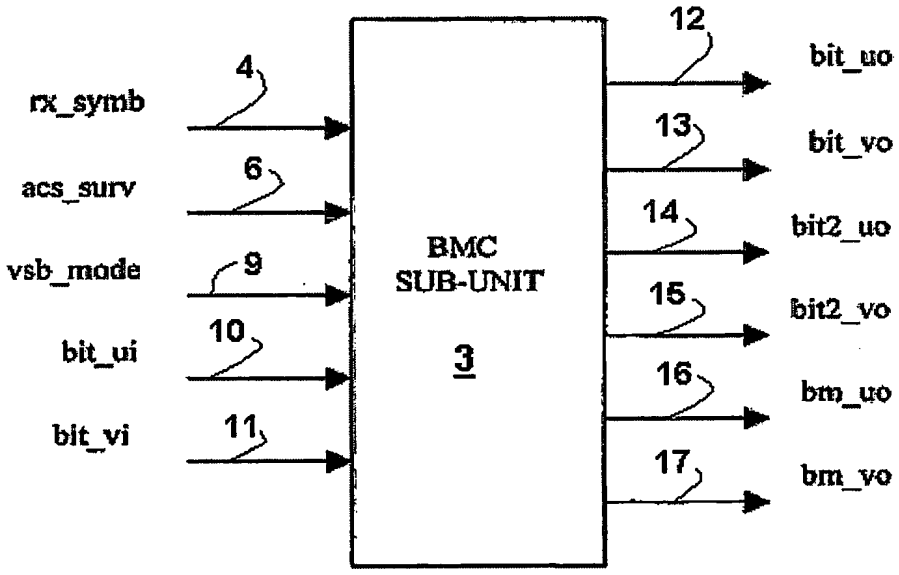

rx_symb
4
acs_surv
6
vsb_mode
9
bit_ui
10
bit_vi
11
BMC SUB-UNIT 3
12
bit_uo
13
bit_vo
14
bit2_uo
15
bit2_vo
16
bm_uo
17
bm_vo

Fig. 10

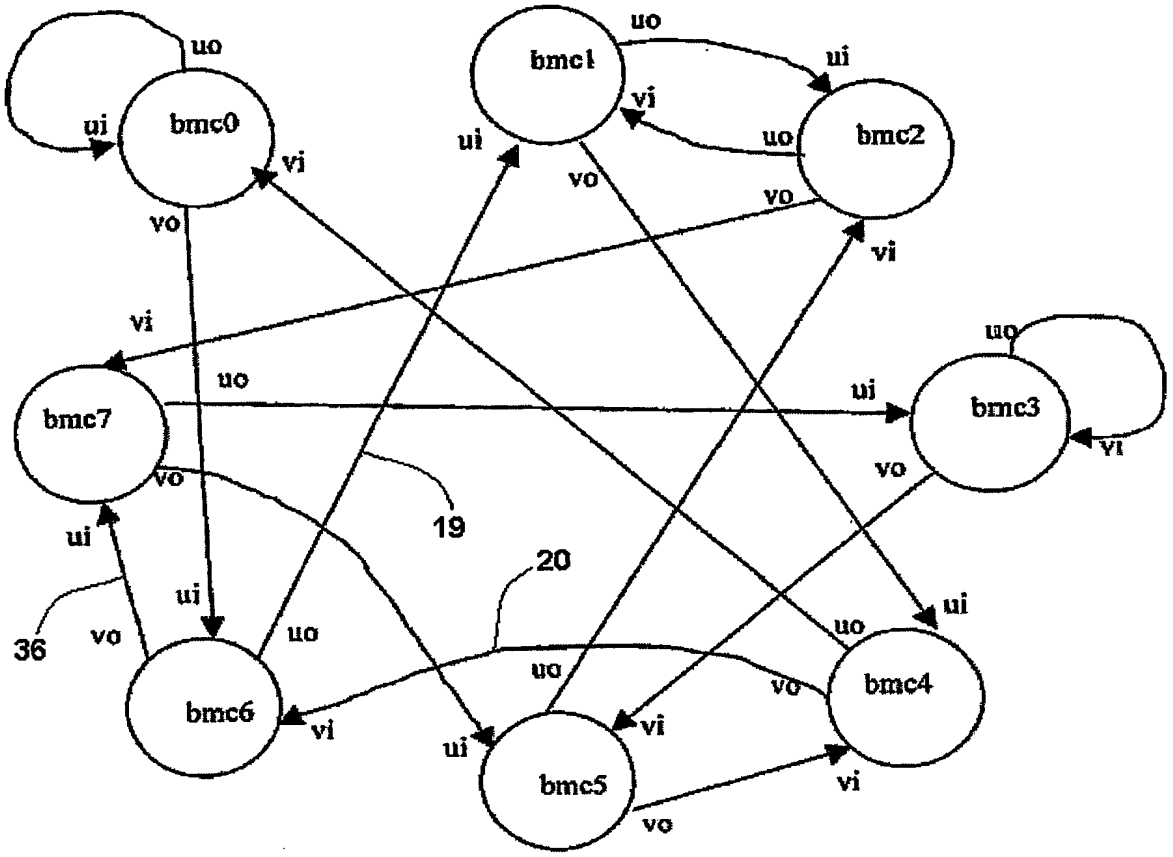


Fig. 11

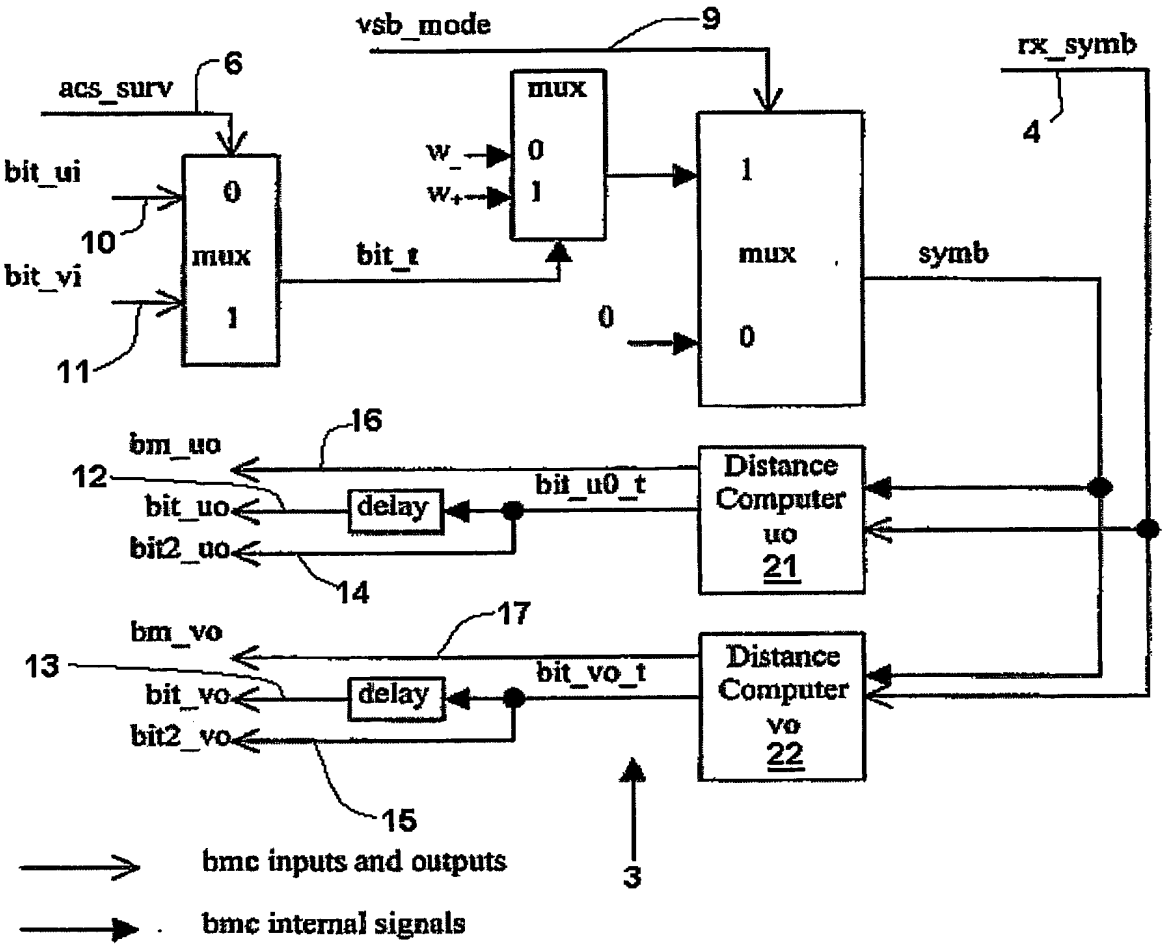
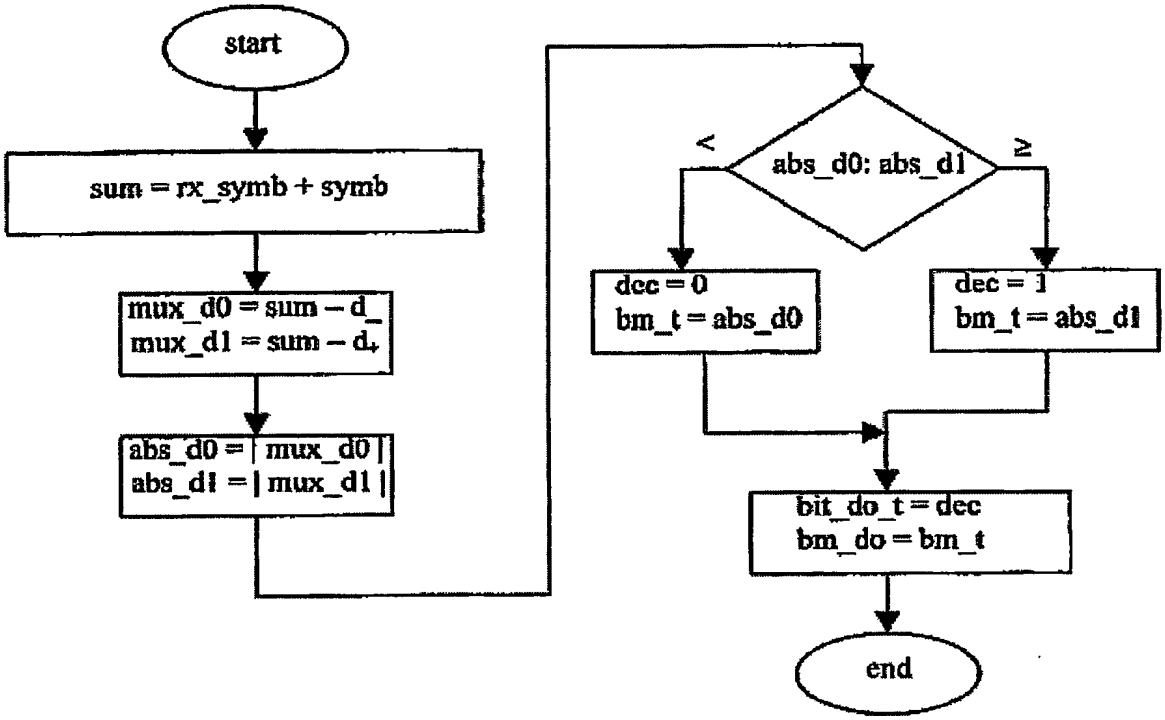

vsb_mode
9
rx_symb
acs_surv
6
4
mux
w_
w+
0
1
bit_ui
10
bit_vi
11
0
mux
1
bit_t
1
mux
0
symb
0
16
bm_uo
12
bit_uo
bit2_uo
delay
bit_u0_t
Distance Computer uo 21
14
17
bm_vo
13
bit_vo
bit2_vo
delay
bit_vo_t
Distance Computer vo 22
15
3
bmc inputs and outputs
bmc internal signals

Fig. 12



Distance computer algorithm do (where u or v can replace d)

Fig. 13

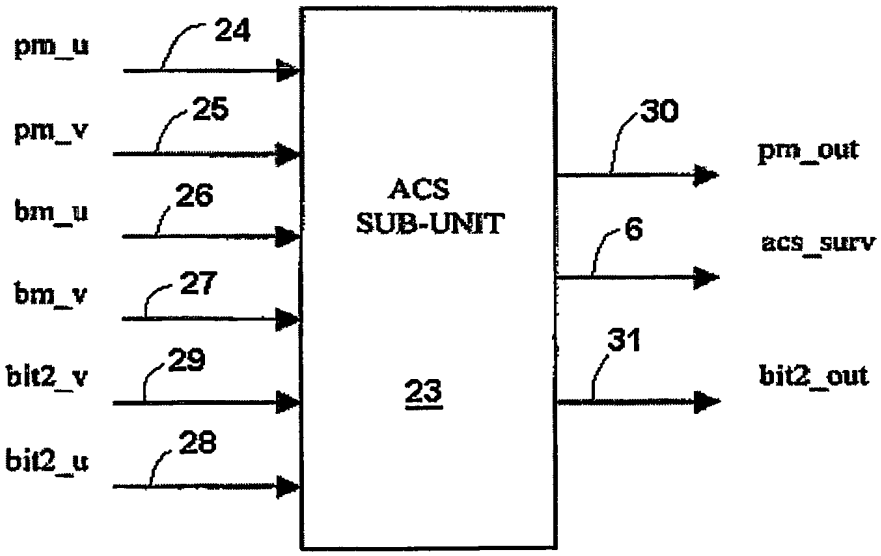


Fig. 14

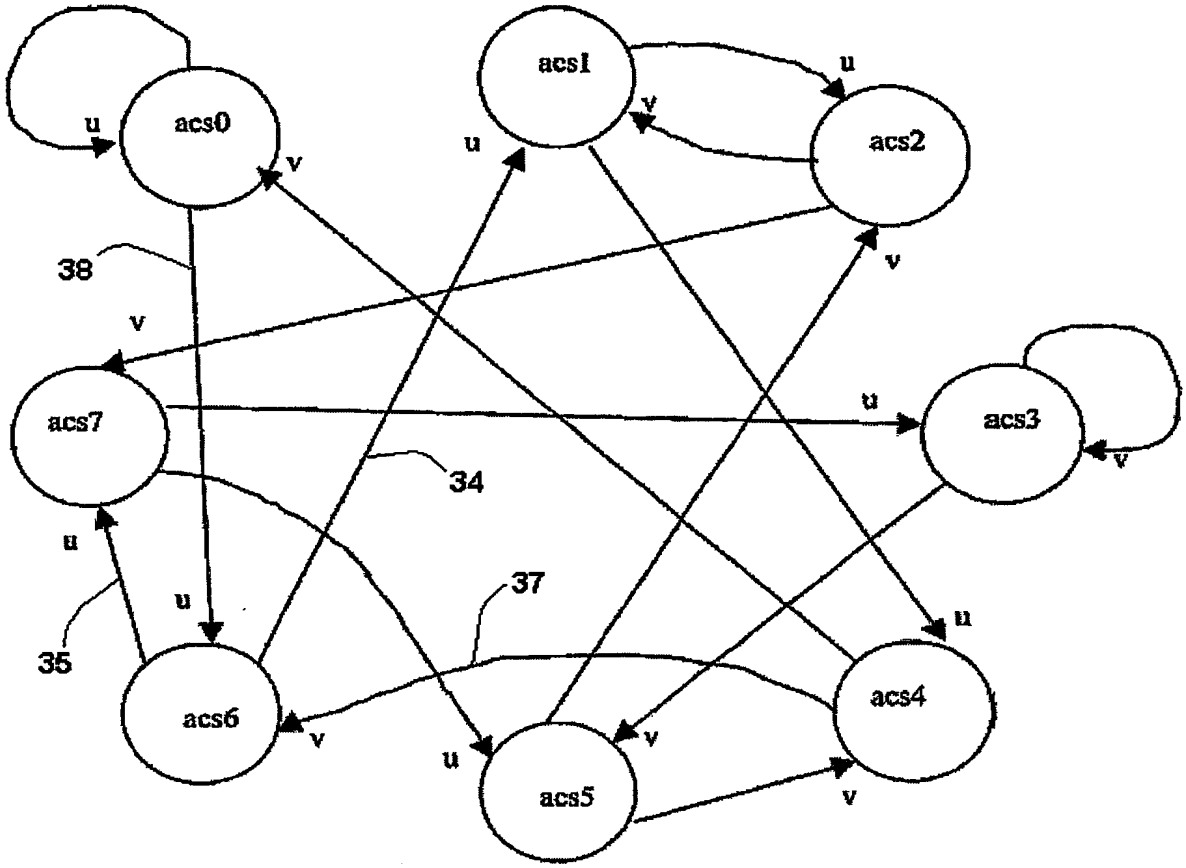

acs0
acs1
acs2
acs3
acs4
acs5
acs6
acs7
u
v
38
34
37
35

Fig. 15

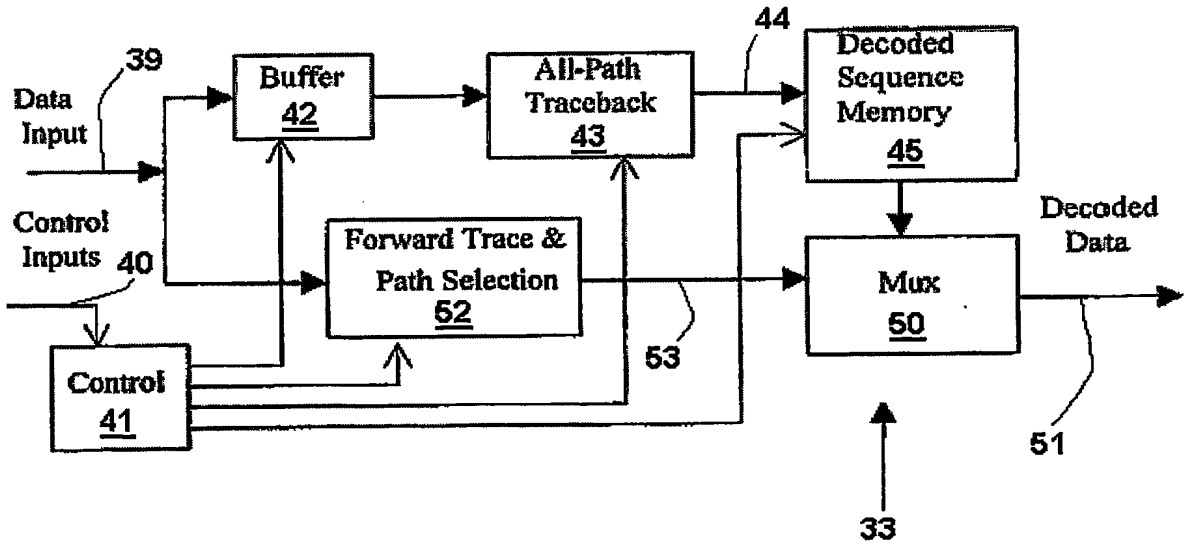

Data Input
39
Buffer 42
All-Path Traceback 43
44
Decoded Sequence Memory 45
Control Inputs
40
Forward Trace & Path Selection 52
Mux 50
Decoded Data
Control 41
53
51
33

Fig. 16

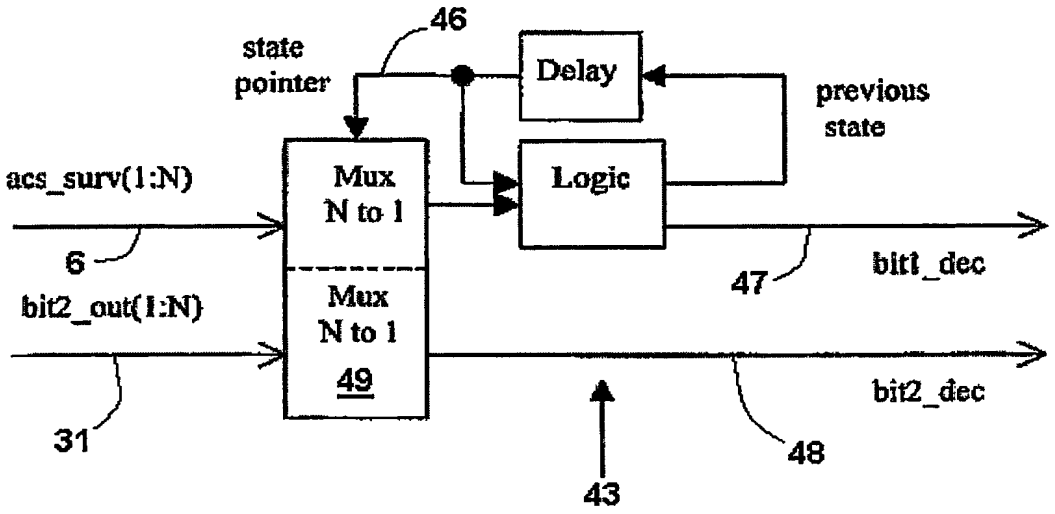

46
state
pointer
Delay
previous
state
acs_surv(1:N)
Mux
N to 1
Logic
6
47
bit1_dec
bit2_out(1:N)
Mux
N to 1
49
bit2_dec
31
48
43

Fig. 17